

POWER REDUCTION IN A MEMORY BUS INTERFACE

ABSTRACT OF THE DISCLOSURE

A technique includes amplifying data signals from a memory bus interface. The amplified data signals are sampled, and the amplifier is selectively disabled in response to
5 the absence of a predetermined operation occurring over the memory bus. In some embodiments of the invention, the amplification may be selectively enabled in response to the beginning of the predetermined operation over the memory bus.

202010-09585001